Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A semiconductor integrated circuit that supplies a plurality of display signals to a corresponding plurality of signal electrodes of an image display apparatus that displays a two-dimensional image, and successively supplies scanning signals to a first group of scanning electrodes and a second group of scanning electrodes of the image display apparatus, the semiconductor integrated circuit comprising:

a storage device that receives and stores image data;

a display signal generation device that generates the plurality of display signals to be supplied to the plurality of signal electrodes based on data stored in the storage device;

a first scanning signal generation device that successively generates scanning signals to be supplied to the first group of scanning electrodes based on a clock signal that defines a scanning timing of the image display apparatus,

wherein each scanning signal enables all of the scanning electrodes on a scanning line,

and wherein the first group of scanning electrodes displays an entire first row of the image;

a second scanning signal generation device that successively generates scanning signals to be supplied to the second group of scanning electrodes based on the clock signal,

wherein each scanning signal enables all of the scanning electrodes on a scanning line,

and wherein the second group of scanning electrodes displays an entire second row of the image; and

a timing control device that generates the clock signal, and generates a first timing control signal for controlling the first scanning signal generation device and a second timing control signal for controlling the second scanning signal generation device such that the first scanning signal generation device and the second scanning signal generation device generate the scanning signals in a specified order,

wherein the first scanning signal generation device outputs a first scanning signal successively to the first group of scanning electrodes based on the first control signal, and

wherein the second scanning signal generation device outputs a second scanning signal successively to the second group of scanning electrodes based on the second control signal.

2. (Original) A semiconductor integrated circuit according to claim 1, wherein the first scanning signal generation device generates the scanning signals to be supplied to the first group of scanning electrodes based on a logical product of the clock signal and the first timing control signal, and the second scanning signal generation device generates the scanning signals to be supplied to the second group of scanning electrodes based on a logical product of the clock signal and the second timing control signal.

3. (Currently amended) A semiconductor integrated circuit that supplies a plurality of display signals to a corresponding plurality of signal electrodes of an image display apparatus that displays a two-dimensional image, and successively ~~supply~~ supplies scanning signals to a first group of scanning electrodes and a second group of scanning electrodes of the image display apparatus, the semiconductor integrated circuit comprising:

a storage device that receives and stores image data;

a display signal generation device that generates the plurality of display signals to be supplied to the plurality of signal electrodes based on data stored in the storage device;

a timing control device that generates a clock signal that defines a scanning timing of the image display apparatus;

a first scanning signal generation device that successively generates scanning signals to be supplied to the first group of scanning electrodes based on the clock signal and a first set potential;

wherein each scanning signal enables all of the scanning electrodes on a scanning line,

and wherein the first group of scanning electrodes displays an entire first row of the image;

a second scanning signal generation device that successively generates scanning signals to be supplied to the second group of scanning electrodes based on the clock signal and a second set potential,

wherein each scanning signal enables all of the scanning electrodes on a scanning line,

and wherein the second group of scanning electrodes displays an entire second row of the image;

wherein the first scanning signal generation device includes a first shift register, a first shift register control circuit that controls the operation of the first shift register, and a first scanning side drive circuit that outputs scanning signals to the first group of scanning electrodes ~~of the liquid crystal panel~~ based on output signals of the first shift register, and

wherein the second scanning signal generation device includes a second shift register, a second shift register control circuit that controls the operation of the second shift register, and a second scanning side drive circuit that outputs scanning signals to the second group of scanning electrodes ~~of the liquid crystal panel~~ based on output signals of the second shift register.

4. (Original) A semiconductor integrated circuit according to claim 3, wherein one of the first and second set potentials is a power supply potential, and the other one is a ground potential.

5. (Currently amended) A semiconductor integrated circuit that supplies a plurality of display signals to a corresponding plurality of signal electrodes of an image display apparatus that displays a two-dimensional image, and successively supply scanning signals to a first group of scanning electrodes and a second group of scanning electrodes of the image display apparatus, the semiconductor integrated circuit comprising:

a storage device that receives and stores image data;

a display signal generation device that generates the plurality of display signals to be supplied to the plurality of signal electrodes based on data stored in the storage device;

a first scanning signal generation device that successively generates scanning signals to be supplied to the first group of scanning electrodes based on a first timing control signal;

wherein each scanning signal enables all of the scanning electrodes on a scanning line,

and wherein the first group of scanning electrodes displays an entire first row of the image;

a second scanning signal generation device that successively generates scanning signals to be supplied to the second group of scanning electrodes based on a second timing control signal;

wherein each scanning signal enables all of the scanning electrodes on a scanning line,

and wherein the second group of scanning electrodes displays an entire second row of the image; and

a timing control device that generates the first and second timing control signals such that the first scanning signal generation device and the second scanning signal generation device generate the scanning signals in a specified order, wherein the timing control ~~circuit~~ device controls output timings of the first

and second scanning signals at the first scanning signal generation device and the second scanning signal generation device, and

wherein the timing control device outputs first pulses to a first line that are clock signals that determine timings for line scanning at the first scanning signal generation device, and outputs second pulses to a second line that are clock signals that determine timings for line scanning at the second scanning signal generation device.

6. (Original) A semiconductor integrated circuit according to any one of claims 1, 3, and 5, wherein the first scanning signal generation device and the second scanning signal generation device alternately generate the scanning signals.

7. (Original) An image display apparatus that displays a two-dimensional image, comprising:

a semiconductor integrated circuit recited in any one of claims 1, 3, and 5;

a panel having the first group and second group of scanning electrodes disposed such that scanning signals to be supplied to the first group of scanning electrodes are input in one direction of the first group of scanning electrodes, and scanning signals to be supplied to the second group of scanning electrodes are input in the other direction of the second group of scanning electrodes; and

a substrate that mounts the panel and the semiconductor integrated circuit thereon.

8. (Original) The semiconductor integrated circuit according to anyone of claims 1, 3, and 5, wherein the first scanning signal generation device comprises:

a first shift register; and

a first driver circuit coupled to the first shift register, said first shift register receiving the clock signal and/or the first timing control signal for successively generating a drive signal to one of a plurality of input terminals of said first driver circuit, said first driver circuit then successively outputting a scanning signal to predetermined scanning electrodes of the first group of scanning electrodes.

9. (Original) The semiconductor integrated circuit according to anyone of claims 1, 3, and 5, wherein the second scanning signal generation device comprises:

a second shift register; and

a second driver circuit coupled to the second shift register, said second shift register receiving the clock signal and/or the second timing control signal for successively generating a drive signal to one of a plurality of input terminals of said second driver circuit, said second driver circuit then successively outputting a scanning signal to predetermined scanning electrodes of the second group of scanning electrodes.

10. (Previously presented) The semiconductor integrated circuit according to claim 3, wherein the first scanning signal generation device comprises a first control circuit for generating a first control signal based on the first set potential, and the second scanning signal generation device comprises a second control circuit for generating a second control signal based on the second set potential, said first and second scanning signal generation device generating scanning signals based on a logical product of the clock signal and the first and second control signals, respectively.

11. (Previously presented) A method for supplying a plurality of display signals and a plurality of scanning signals to an image display apparatus from a semiconductor integrated circuit, the method comprising the steps of:

receiving image data by the semiconductor integrated circuit;

generating the plurality of display signals based on the image data and supplying the plurality of display signals to signal electrodes of the image display apparatus;

generating first and second control signals respectively for first and second drivers of the semiconductor integrated circuit;

alternately generating scanning signals by the first and second drivers based on the first and second control signals; and

supplying the scanning signals in succession to scanning electrodes of the image display apparatus;

wherein each scanning signal enables all of the scanning electrodes on a scanning line, and

wherein a first group of the scanning electrodes displays an entire first row of an image and a second group of the scanning electrodes displays an entire second row of the image.

12. (Original) The method according to claim 11, wherein the step of generating first and second control signals comprises:

generating a clock signal; and

alternately generating the first and second control signals based on the clock signal.

13. (Original) The method according to claim 11, wherein the step of generating first and second control signals comprises:

generating a clock signal; and

alternately generating first and second timing control signals, said first and second drivers generating the scanning signals based on a logical product of the clock signal and the first and second timing control signals, respectively.

14. (Original) The method according to claim 11, wherein the step of generating first and second control signals comprises:

generating a clock signal; and

alternately generating first and second timing control signals respectively based on a first and a second set potential, said first and second drivers generating the scanning signals based on a logical product of the clock signal and the first and second timing control signals, respectively.

15. (Original) The method according to claim 14, wherein the first set potential is a power supply potential and the second set potential is a ground potential.